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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,167	04/08/2004	Dong-Hyuk Chae	4591-390	2938

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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,167	CHAE ET AL.	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/31/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Updated Search History*.

DETAILED ACTION

1. This communication is responsive to the following communications: the Amendment after Non-Final Rejection, filed on January 31, 2006.

2. Claims 1-21 are pending in the application. Claims 1, 7, 13, and 19 are independent claims.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. KR 2003-21969, filed on April 8, 2003, and parent Application No. KR 2003-79510, filed on November 11, 2003.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2, 5, 7-8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of the US Patent to Oguchi (4,356,482), and further in view of the US Patent to Okumura et al. (6,289,411).

2. **Regarding claims 1-2, 7-8,** the AAPA discloses, in Fig. 2, a memory system comprising a memory cell array **60** constructed of a plurality of sectors; a register circuit **10** to store a loaded sector information about a sector to be erased; a counter **30** to

generate an address including a chip information and a sector information and that generates addresses in sequence; a control circuit **40** to generate an address count-up signal with reference to that sector information corresponds to a sector to be erased that has chip selection information to check the sector information when the chip selection information is identical to the chip information of the counter; and a core driver **50** that carries out an erase operation for a corresponding sector in response to the erase enable signal (paragraphs 0008, 0011). The AAPA does not disclose an address clock driver to generate an address clock signal in response to the disclosed current chip signal and address count-up signal, nor does it disclose that there is a plurality of memory chips with a current chip signal that activates a currently selected chip from a plurality of memory chips. Oguchi teaches a memory system with an address clock generator **26** comprising a decoder **26b** that generates an address clock signal in response to an address count-up signal from counter **26a**. It is maintained from the previous office action it is obvious that if one can use the circuitry to connect to one chip, you can connect to a plurality of chips (duplication of parts involves only routine skill in the art; *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8). However, Oguchi also teaches that his memory system can be employed by multiple memory chips as well as in a single chip (column 10, lines 20-26). Other circuitry similar to the field of endeavor includes a memory array **50**, and a refresh address counter **36** to generate an address including sector information. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the address clock driver of Oguchi with the circuitry of the AAPA, manifested in a plurality of chips, for the purpose of more

accurately controlling the input and output of data to certain addresses. Okumura et al. teach a controller circuit for generating a chip select signal to select and activate a chip from a plurality of memory chips. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the control circuit of Okumura et al. to control the combined circuitry of Oguchi and the AAPA manifested in a plurality of chips, as taught by Oguchi, due to the fact that if there is a plurality of chips, there must be some sort of controller to select the chips, and the CPU of Oguchi can be exchanged for the CPU of Okumura et al to achieve this desired effect.

3. Claims 3, 9, 13-15, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of US Patent to Oguchi (4,356,482) and the US Patent to Okumura et al. (6,289,411), and further in view of the US Patent to Fling (4,654,695).

4. **Regarding claims 3, 9, 13-15, and 17,** the AAPA, Oguchi, and Okumura et al. teach all the claimed elements as discussed above, but fail to explicitly teach an output of an address clock driver conditioned at a high impedance state when the chip selection information is different from the chip information of the counter, a first bus to transfer control signals, a second bus to transfer address and data signals, a plurality of memory chips connected to these buses. Fling teaches, in Fig. 1, an address clock driver **26** that generates an address clock signal. He also teaches that this address clock signal provides a high impedance state when it is in a low state to a first bus that transfers control signals to a memory **22**, and a second bus that that transfers the address and data signals to a memory **22**. It would have been obvious to use the

circuitry and signals described by Fling to connect to a plurality of memory chips, as it is obvious that if you can use the circuitry to connect to one chip, you can connect to a plurality of chips (duplication of parts involves only routine skill in the art; *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8). Furthermore, even though Fling fails to explicitly say his circuitry can be implemented in a plurality of chips, Oguchi teaches a similar address clock driver implemented in a plurality of chips, and Okumura et al. teach a way to control a plurality of chips. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to use the address clock driver described by Fling in the system described by the AAPA, Oguchi, and Okumura et al. for the purpose of more accurately controlling the writing and erasing of data to certain addresses, and to use the busses described by Fling to transfer control, address, and data signals to the plurality of chips.

5. Claims 4, 10, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of US Patent to Oguchi (4,356,482), the US Patent to Okumura et al. (6,289,411), and the US Patent to Fling (4,654,695), and further in view of the US Patent to Peri et al (6,904,400).

6. **Regarding claims 4, 10, and 16,** the AAPA, Oguchi, Okumura et al., and Fling teach all the claimed elements but fail to teach where the chip selection information is established by a hard-coded option. Peri teaches, in claims 15 and 24, a state machine or control circuit that can load addresses, which can be hard-coded, into a register. It would have been obvious to one of ordinary skill of the art at the time the invention was

made to implement the hard-coded option taught by Peri into the system taught by the AAPA, Oguchi, Okumura et al., and Fling because it would give the user the option to tell the system directly which addresses he wanted to put the data into.

7. Claims 6, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of US Patent to Oguchi (4,356,482), the US Patent to Okumura et al. (6,289,411), and the US Patent to Fling (4,654,695), and further in view of the US Patent to Fukumoto (5,488,587).

8. **Regarding claims 6, 12, and 18,** the AAPA, Oguchi, Okumura et al., and Fling teach all the claimed elements as discussed above but fail to teach the chip information of a counter corresponding to a most significant address bit. Fukumoto teaches, in column 16, lines 42-44, chip information of a counter corresponding to a most significant address bit. It would have been obvious to one of ordinary skill of the art at the time the invention was made to combine the teachings of Fukumoto with the system of the AAPA, Oguchi, Okumura et al., and Fling because it is an effective way of determining the correct address in which to write or erase the data.

9. **Regarding claims 19-21,** they encompass the same scope of invention as that of claims 1-18 except they draft the invention in method format instead of apparatus format. The AAPA and Fling teach all the circuitry necessary to erase multi-sectors in a multi-chip package. Peri and Fukumoto teach all the necessary options needed to navigate the address sectors in an orderly and accurate fashion. The aspects of the invention contained in claims 19-21 are therefore rejected in method format for the

same reasons claims 1-18 were rejected in apparatus format, as set forth in the above paragraphs of the office action.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin (5,526,316) discloses a memory system that uses address clock signals to input to a counter to generate address and sector information. Schofield (5,570,381) discloses the use of the most significant address bit in a counter. Ramamurthy et al. (5,848,026) teach the use of clock drivers and address counters and registers to select a specific block of memory cells. Lepejian et al. (5,974,579) teaches a memory system with a system including an address clock driver, an address-generating counter, and a control circuit to provide address and sector information, which controls multiple memory arrays or blocks.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
3/21/06

3/31/06

TUAN T. NGUYEN
PRIMARY EXAMINER